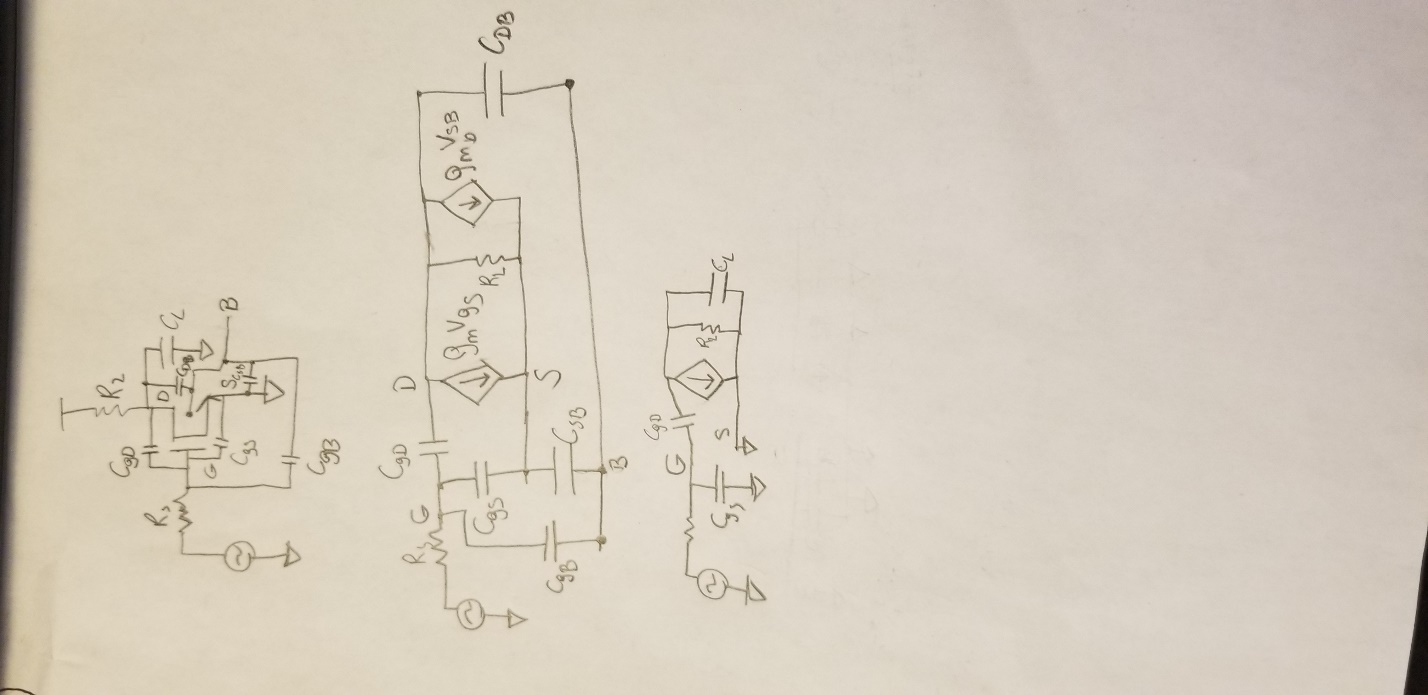
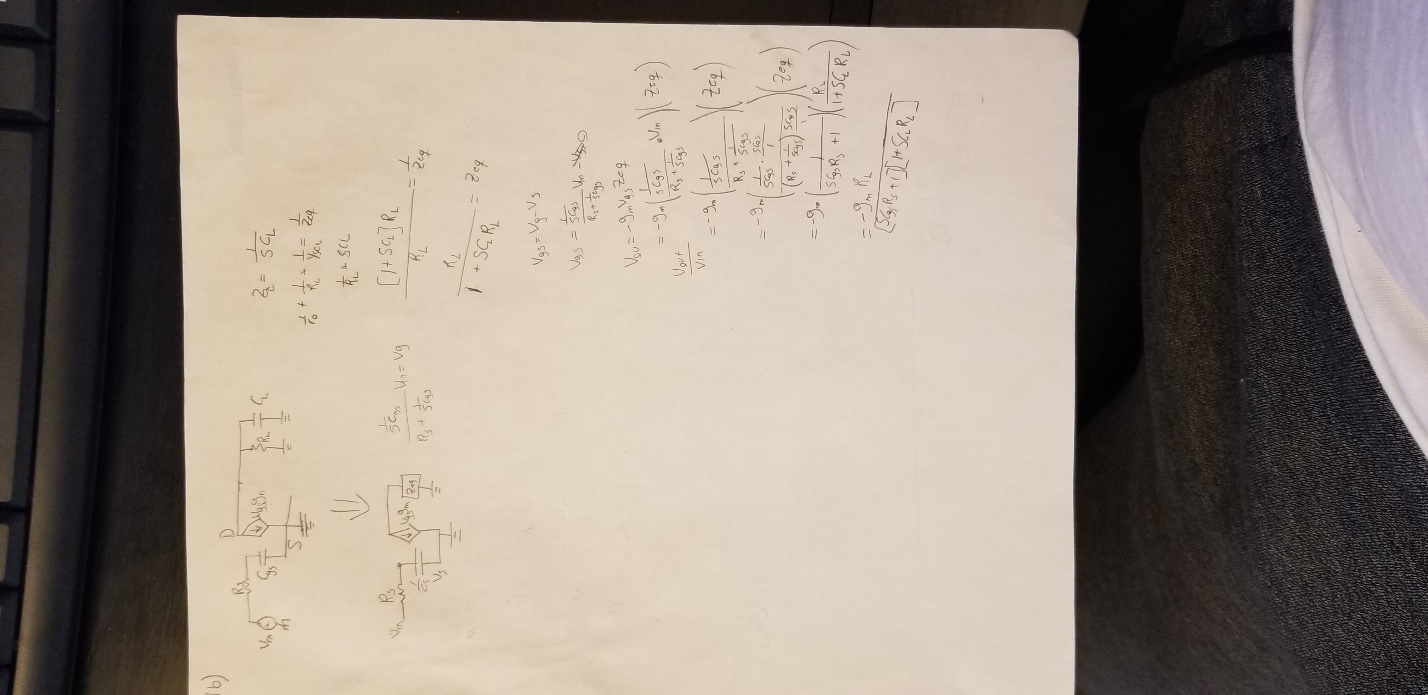
EE 223 HW2

Enrique Hernandez

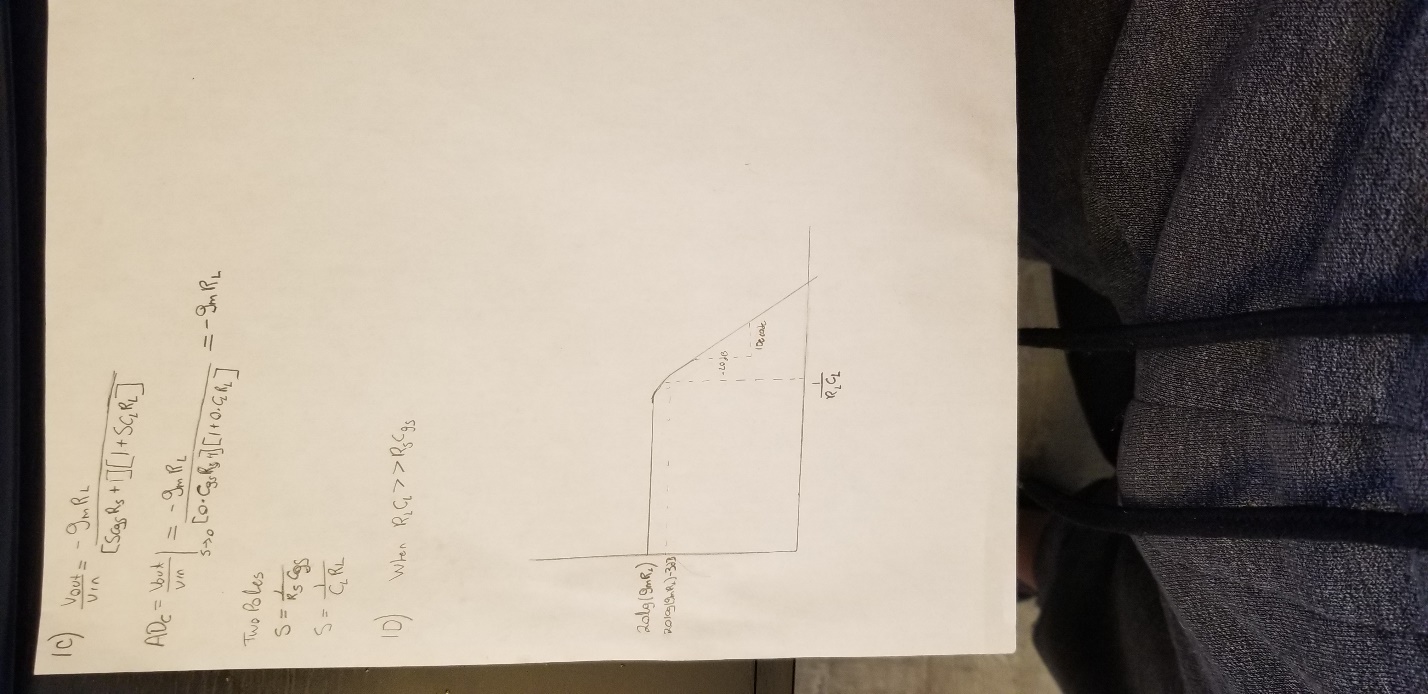
09/29/2018

1. MOS Small-Signal Analysis on Common Source Amplifier





C.



1. Cadence Spectre Simulation of Common-Source Amplifiers
   1. Schematic and simulation

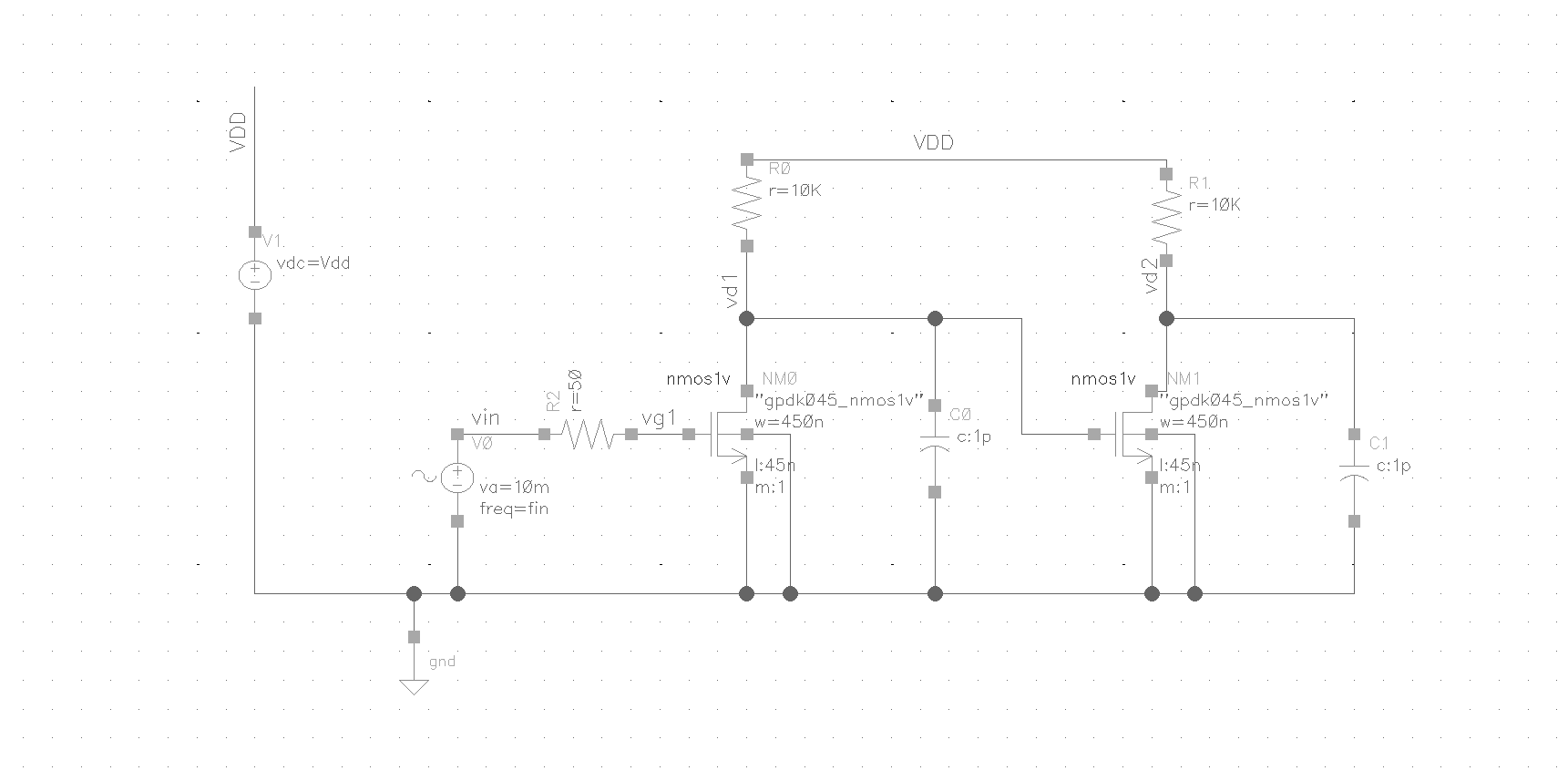


Figure 1: Schematic

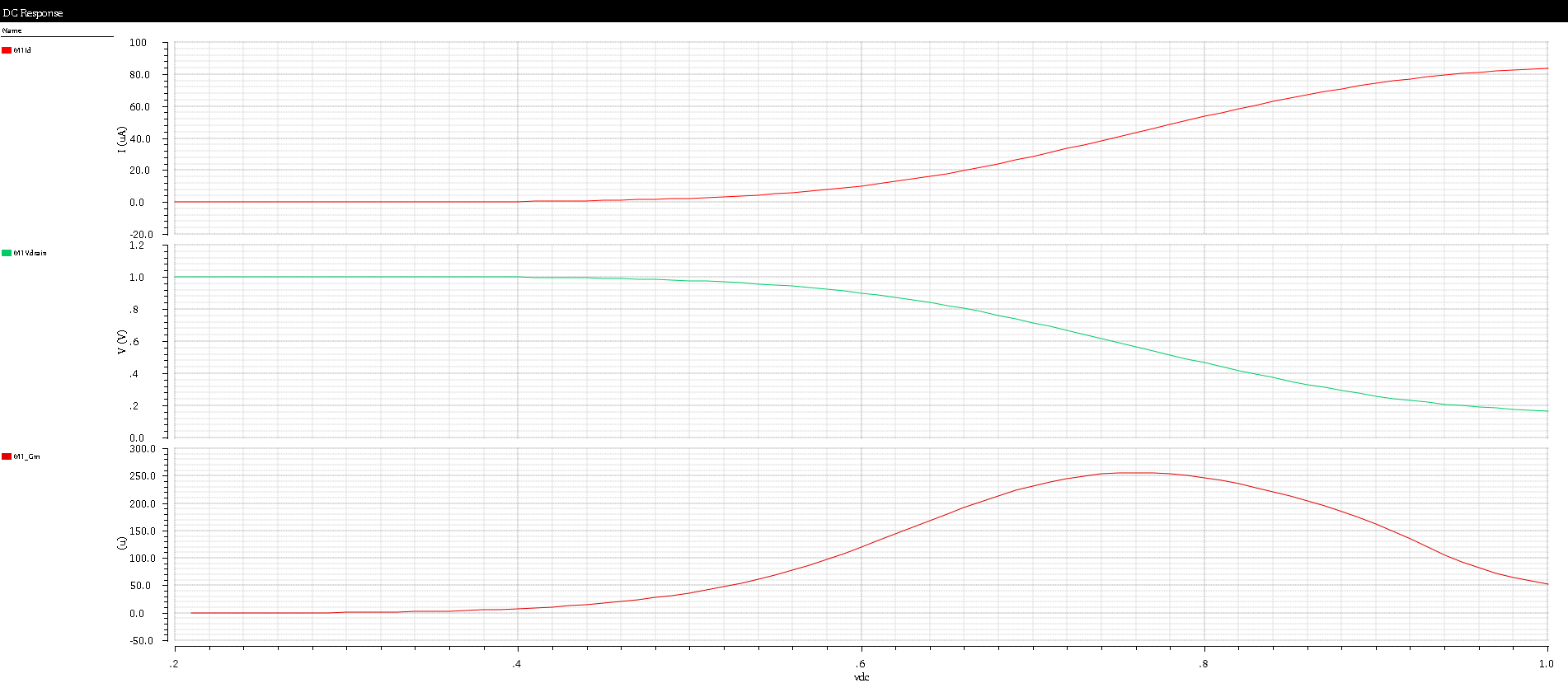
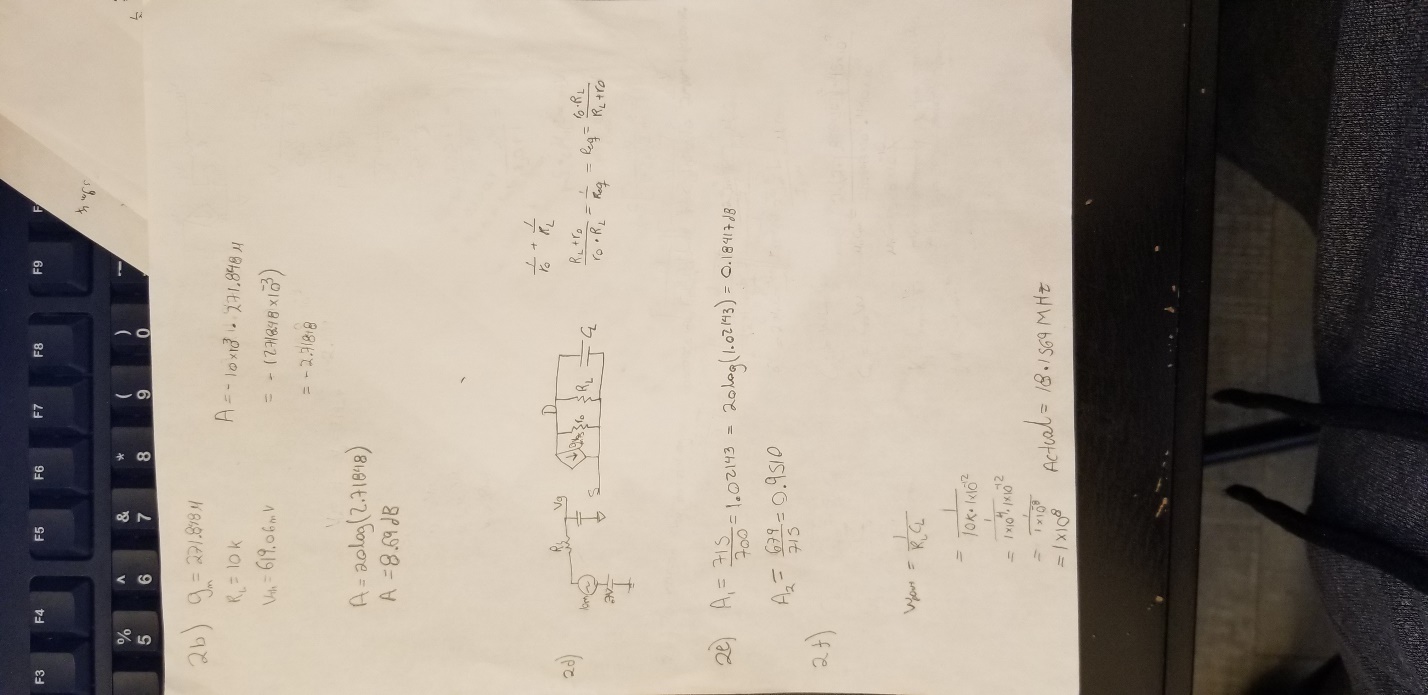


Figure 2: Red curve is Id vs Vg, Green curve is Vd vs Vg and Orange curve is Gm vs Vg.

B.



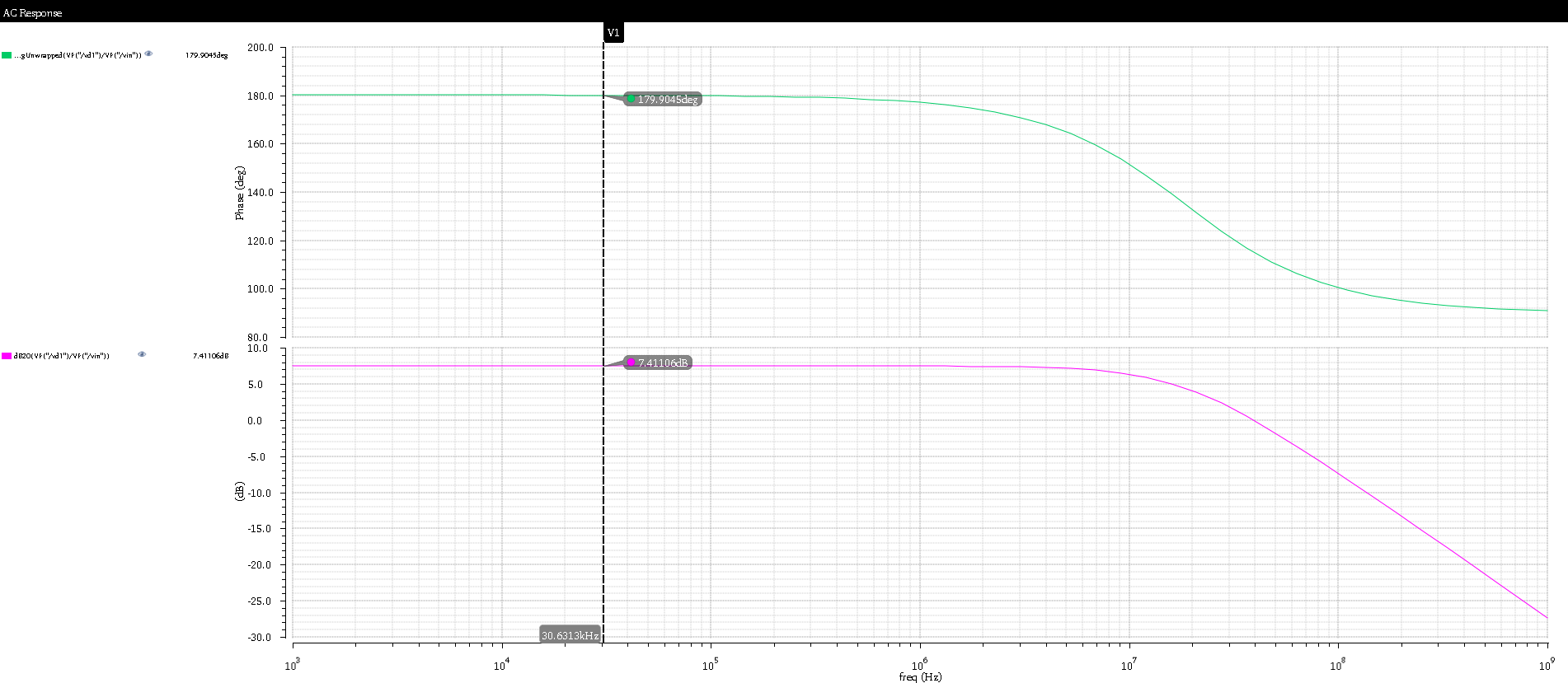


Figure 3: Gain Vs Frequency (pink trace)

* 1. The reason the calculated result and the simulated result do not agree is because the ro is not infinity. There is a channel length modulation that causes a gain change. This is because ro is in parallel with the load resistance causing the gain to be smaller.

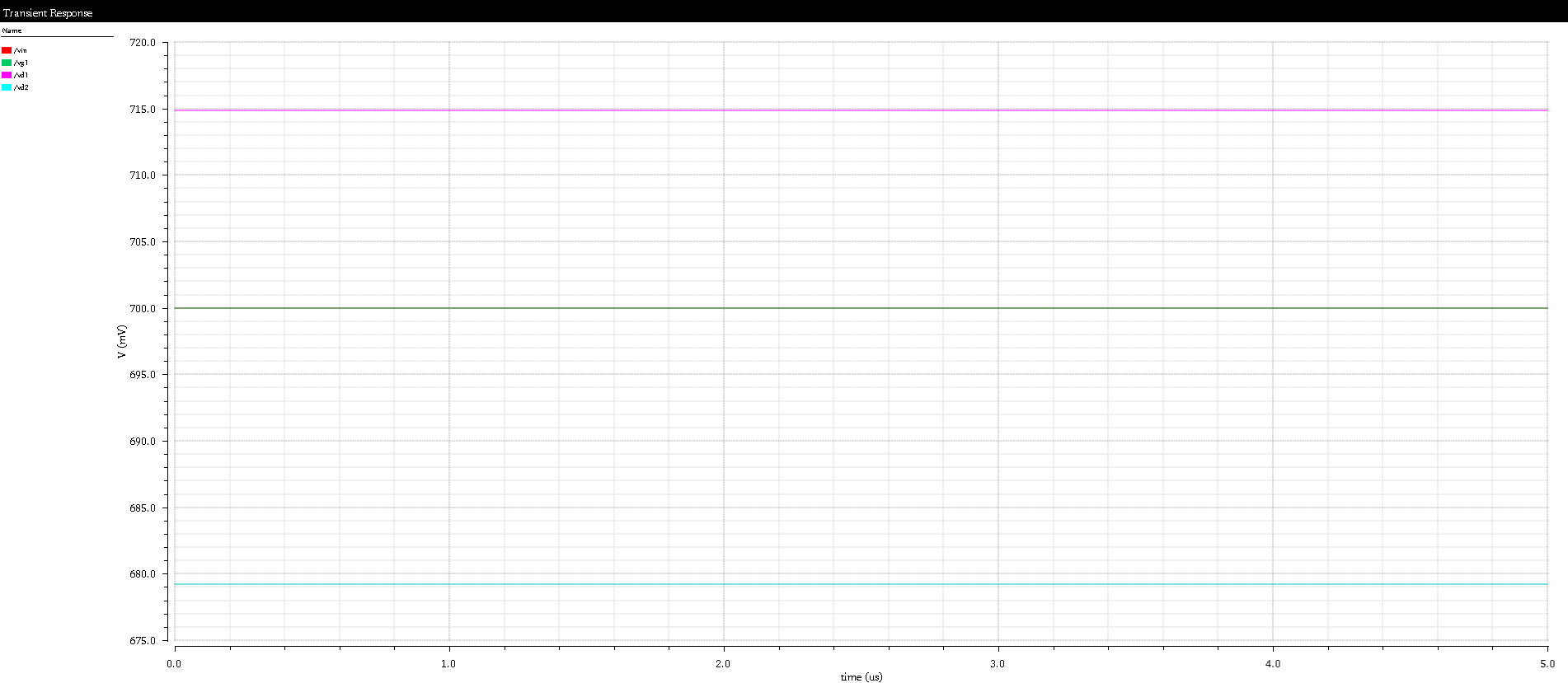


Figure 4: Transient simulation for Vin (Green), Vd1(pink) and Vd2(blue)

* 1. The results of the calculated poles and the simulated poles do not agree is because the output capacitance is not only the load capacitor. There are other capacitances that contribute to the output capacitance. This causes the pole to take effect at a smaller frequency.

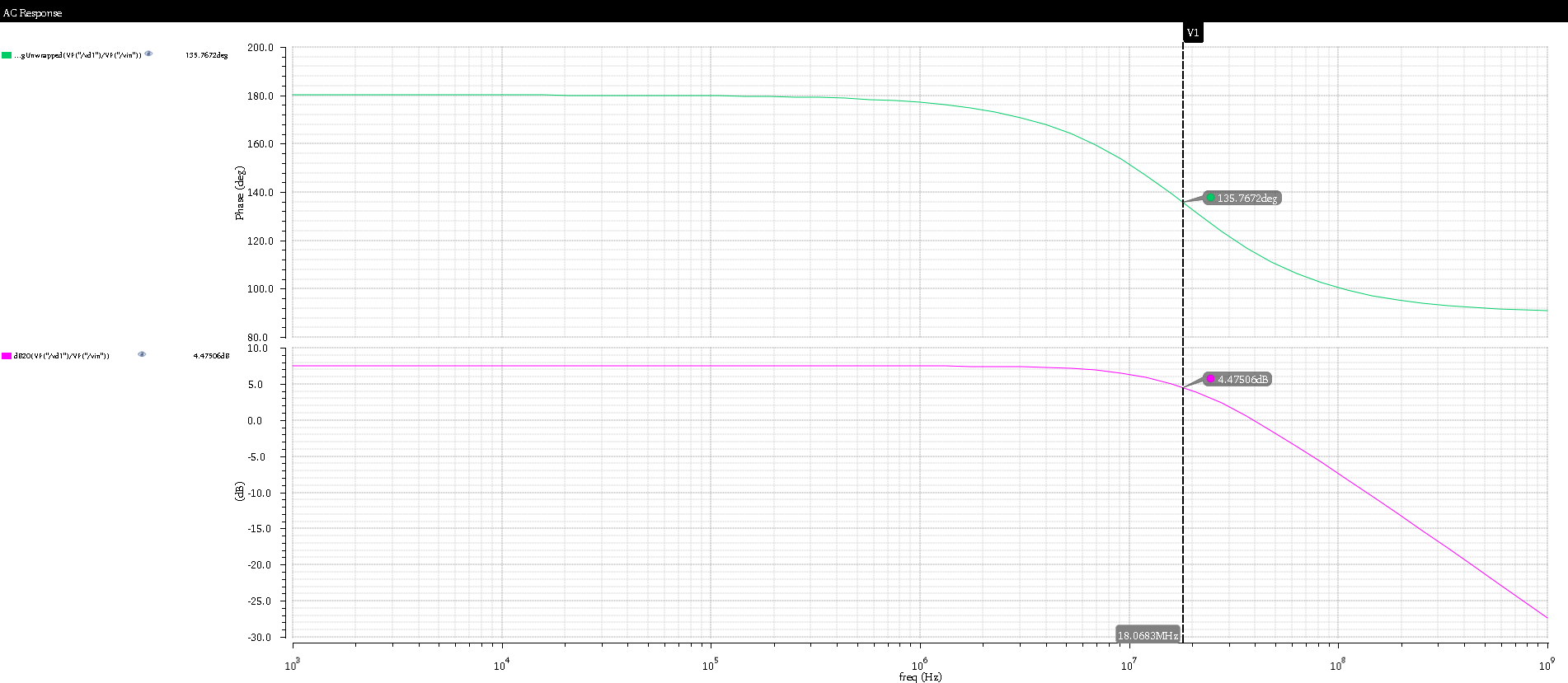
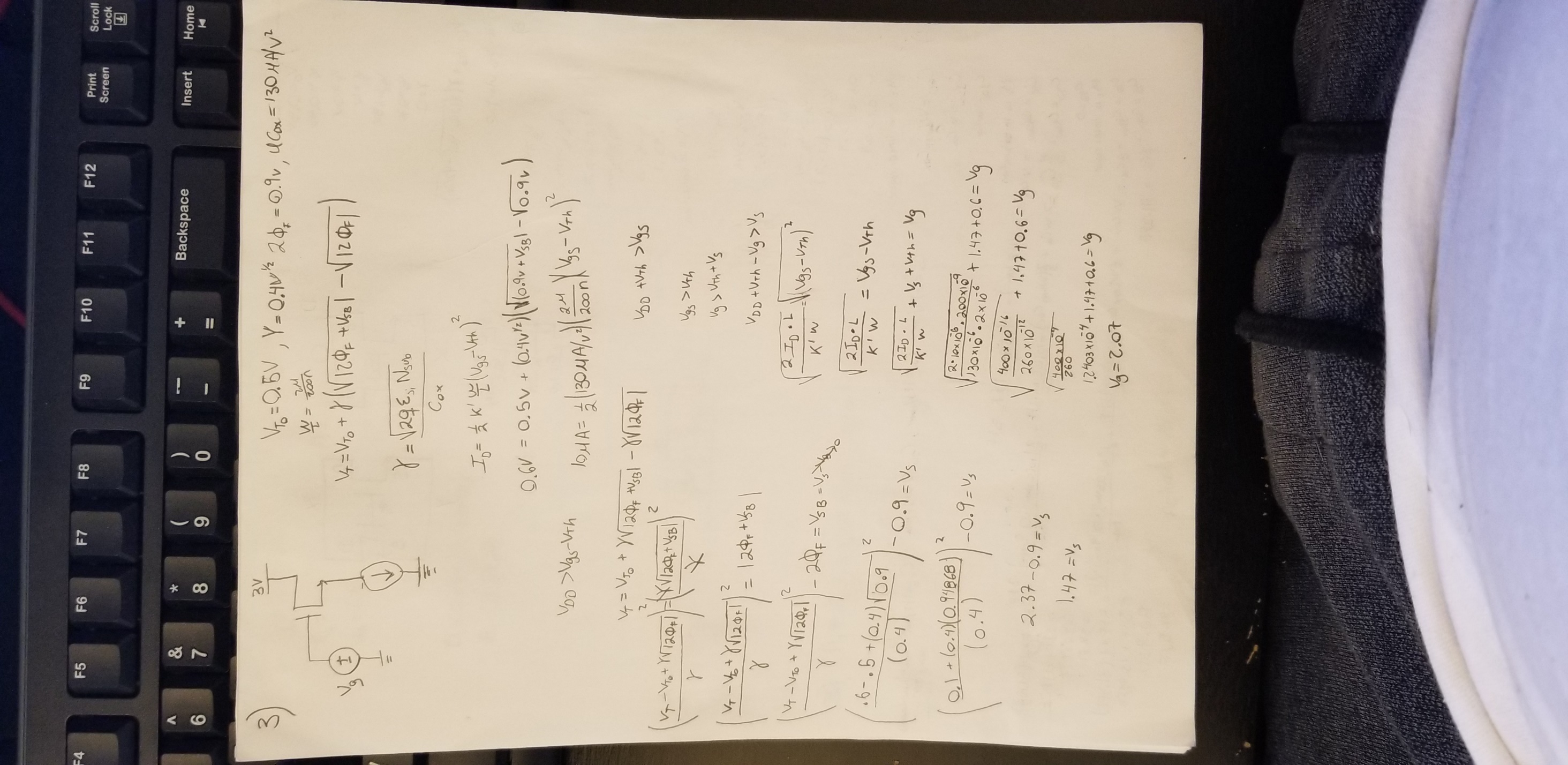


Figure 5: transfer function 3dB point (simulate 18MHZ, Calculated 100MHZ)

1. Body Effect on Threshold Voltage



1. Layout & Transistor Capacitors

